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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,421	03/25/2004	Masafumi Takahashi	251020US2	5331

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EXAMINER	
RADOSEVICH, STEVEN D	
ART UNIT	**PAPER NUMBER**
2117	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	04/09/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 04/09/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/808,421	TAKAHASHI ET AL.	
	Examiner	Art Unit	
	Steven D. Radosevich	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *5-7* is/are allowed.

6)☒ Claim(s) *1-4 and 8* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-8 are present for examination within this instant response.

Priority

Acknowledgement is made that foreign priority is claimed for this application and as such the date (03/26/203) is being used for this examination.

Information Disclosure Statement

Acknowledgement is made that an IDS was provided and has already been reviewed within the prior examination of the application.

Drawings

The drawings are objected to because after reviewing the applicant's remarks figures 3-5 do not illustrate the intended conversion of serial-to-parallel data as indicated within the last paragraph on page 7 of the applicants remarks filed on 12/26/2006 used to support applicant's remarks regarding claim 6 and it's prior 35 U.S.C. 112 second paragraph rejection. Examiners suggests that the output of the serial-to-parallel converter within each figure have a backslash throw it to indicate a plurality of outputs so as to indicate serial-to-parallel conversion by the converter within each figure over the present three inputs resulting in a single output supporting an understanding on parallel-to-serial conversion. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be

labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

Claims 1, 2, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) and further in view of Kim et al (U.S. Patent 5504756).

1. As per claim 1, AAPA teaches A logic circuit having a self-test function comprising:

> A plurality of scanning flip-flops (F/F) circuits having at least a first-stage scanning F/F circuit, a second-stage scanning F/F circuit and a last-stage scanning F/F circuit, each having a clock input terminal, a scanning input terminal and a scanning output terminal, the scanning F/F circuits being connected one another so that a scanning clock signal is input to the clock input terminal of each scanning F/F circuit and a signal output from the scanning output terminal of the

first-stage scanning F/F circuit is supplied to the scanning input terminal of the second-stage scanning F/F circuit for sequential logical operations (figure 6 with pages 1-2 lines 33-33);

AAPA does not specifically teach:

The plurality of scanning F/F with a feed-back signal line connecting the output of the last-stage scanning F/F to the input of the first-stage scanning F/F;

At least one data selector selecting either an external scanning signal or the signal fed back form the last-stage scanning F/F to be supplied to the input terminal of the first-stage scanning F/F;

At least one scanning controller supplying a control signal to the data selector to select which signal supplied to the data selector is supplied to the input terminal of the first-stage F/F; and

An external scanning output terminal via which the signal fed back from the last-stage scanning F/F circuit is output from the logic circuit.

However within an analogous art Kim teaches a scanning F/F with a feed-back signal line connecting the output of the last-stage scanning F/F to the input of the first-stage scanning F/F (figures 3 and 10a, Column 2 lines 22-34, 44-45, and 51-54); at least one data selector selecting either an external scanning signal of the signal fed back from the last-stage scanning F/F to be supplied to the input terminal of the first stage-scanning F/F (figures 3 and 10a, column 2 lines 55-64 and column 4 lines 11-18); at least one scanning controller supplying a control signal to the data selector to select

which signal supplied to the data selector is supplied to the input terminal of the first-stage F/F (figures 3 and 10a, column 3 lines 44-50 with column 4 lines 17-55); and an external scanning output terminal via which the signal fed back from the last-stage scanning F/F circuit is output form the logic circuit (figures 3 and 10a and column 4). Examiner notes that a controller or CPU is required to supply the control signals within any circuit or circuitry.

Therefore it would have been obvious to one of ordinary skill within the art at the time the invention was made to have been motivated to combine the AAPA scan chain configuration with the feed-back line, data selector, scanning controller, and output terminal as described above in detail so as to provide a multi-frequency, multi scan chain as indicated within Kim (column 3 lines 40-50).

2. As per claim 2, Kim teaches the scanning controller supplies the control signal to the data selector based on a processor instruction of a prestored program (column 4 lines 17-55).

3. As per claim 8, AAPA as modified with Kim teaches the logic circuit comprising: a F/F scan chain (plurality of scanning flip-flops (F/F) circuits), a feed-back signal line, at least one data selector, at least one scanning controller, and an external output terminal as described above in detail.

AAPA as modified with Kim does not specifically teach wherein the scanning F/F circuits are divided into a plurality of logic groups each including the data selector, the clock selector, and the scanning controller.

AAPA as modified with Kim teaches the logic circuit comprising: a F/F scan chain (plurality of scanning flip-flops (F/F) circuits), a feed-back signal line, at least one data selector, at least one scanning controller, and an external output terminal as described above in detail. It would have been obvious to one having ordinary skill within the art at the time the invention was made to have multiple identical scanning F/F or scan chains/groups comprising multiple scanning F/F each including the data selector, the clock selector, and the scanning controller, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.,* 193 USPQ 8.

Therefore it would have been obvious to one of ordinary skill within the art at the time the invention was made to have multiple identical scanning F/F or scan chains/groups comprising multiple scanning F/F each including the data selector, the clock selector, and the scanning controller since it is well known that multiple groups have scanning F/F can execute testing faster then one single group of scanning F/F.

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA as modified with Kim as applied to claim 1 and 2 above, and further in view of Johnson (U.S. Patent 4811345) and Sagawa et al (U.S. Patent 3872245).

4. As per claim 3, AAPA as modified with Kim teaches a logic circuit comprising: a F/F scan chain (plurality of scanning flip-flops (F/F) circuits), a feed-back signal line, at least one data selector, at least one scanning controller, and an external output terminal as described above in detail.

AAPA as modified with Kim does not specifically teach the processor instruction is a reduced instruction set computer instruction.

However within an analogous art Johnson teaches reduced instruction set computer (RISC) architectures within testing, wherein RISC architecture have simplified instruction sets and simplified bus structures (columns 1-2 lines 63-11). The art is replete with references teaching RISC architecture within testing.

Therefore it would have been obvious to one of ordinary skill within the art at the time the invention was made to have been motivated to combine the AAPA as modified with Kim logic circuit with the RISC architecture of Johnson to take advantage of the simplified instruction sets and bus structure to allow easy debugging and construction of the circuitry.

5. As per claim 4, AAPA as modified with Kim teaches a logic circuit comprising: a F/F scan chain (plurality of scanning flip-flops (F/F) circuits), a feed-back signal line, at least one data selector, at least one scanning controller, and an external output terminal as described above in detail.

AAPA as modified with Kim does not specifically teach at least one clock selector to select either an external scanning clock signal or an internal scanning clock signal supplied from the scanning controller, the selected scanning clock signal being supplied to the clock input terminal of each scanning F/F circuit; and an external clock output terminal via which the selected scanning clock signal supplied to the clock input terminal of each scanning F/F circuit is output from the logic circuit.

However within an analogous art Sagawa teaches at least one clock selector to select either an external scanning clock signal or an internal scanning clock signal supplied from the scanning controller, the selected scanning clock signal being supplied to the clock input terminal of each scanning F/F circuit; and an external clock output terminal via which the selected scanning clock signal supplied to the clock input terminal of each scanning F/F circuit is output from the logic circuit (Sagawa – column 5 lines 10-15) The art is replete with references wherein selection of an external clock or internal clock is done.

Therefore it would have been obvious to one of ordinary skill within the art at the time the invention was made to have been motivated to combine the AAPA as modified with Kim logic circuit with the clock selection and output of Sagawa to allow both operating synchronization between communicating circuits and allow non-synchronization of circuits wherein one circuit can operate at a faster speed then another when communication is not required between circuits, thus reducing total processing time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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